

IN THE SPECIFICATION

Replace paragraph [0042] as follows:

[0042] Within write buffer/ECC generator 105, the WBHit signal is applied to input terminals of OR gates 206 and 207. Thus, when the WBHit signal is asserted high, OR gate 206 provides a logic high signal to the clock input terminal of register 201. Consequently, the write data, write address and associated check bits stored in input register 201 are latched into output register ~~201~~ 200 at this time. OR gate 207 provides a logic high signal to flip-flop 208. This logic high signal is latched into flip-flop 208 in response to the rising edge of the CLK signal. Tri-state output buffers 210 and 211 are enabled in response to the logic high signal latched into flip-flop 208. As a result, the data value and the corresponding ECC value stored in output register 201 are driven onto data bus MD[71:0]. The data and ECC values on data bus MD[71:0] are routed to error detection/correction unit 106. In response, error detection/correction unit 106 provides a corrected data value, which is routed through output driver 108 to data output bus Do[63:0], thereby completing the read access.

Replace paragraph [0054] as follows:

[0054] The logic high RESET signal also sets the read pointer value RP provided by toggle flip-flop 313 to a logic "1" value, such that multiplexers 341-343 are initially set to pass the CCB₁, CD₁ and LA₁ values, respectively, from register ~~300~~ 301.